

PATENT

IN THE UNITED STATES PATENT OFFICE

Applicants: Jason H. Anderson et al.
Assignee: Xilinx, Inc.
Title: Post-Layout Optimization in Integrated Circuit Design
Serial No.: 10/644,132 File Date: 08/20/2003
Examiner: Binh C. Tat, Art Unit: 2825
Docket No.: X-946 US Conf. No.: 5337

Mail Stop AMENDMENT
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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. 1.56, Applicants bring to the attention of the Examiner the three (3) references listed in the attached Substitute for Form 1449A/PTO. A copy of each is enclosed herein.

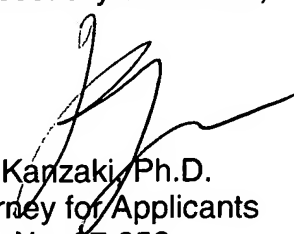
The enclosed reference(s) is/are being cited after the receipt of a first office action but prior to any final action.

Citation of the above documents shall not be construed as an admission that the documents are necessarily prior art with respect to the instant invention. Citation of the above documents shall not be construed as a representation that a search has been made other than as described above. Also, the citation of the above documents shall not be construed as an admission that the information cited herein is, or is considered to be, material to patentability as defined in §1.56(b).

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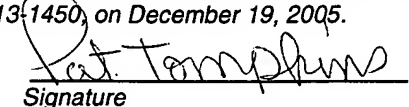
Respectfully submitted,

12/23/2005 DTESSEM1 00000016 240040 10644132
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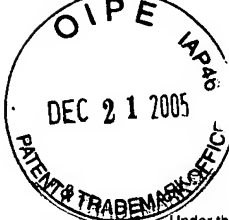

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on December 19, 2005.

Pat Tompkins
Name


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Substitute for form 1449A/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application / Conf. No.	10/644,132 / 5337
		Filing Date	August 20, 2003
		First Named Inventor	Jason H. Anderson
		Art Unit	2825
		Examiner Name	Binh C. Tat
Sheet	1 of 1	Attorney Docket Number	X-946 US

OTHER -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		C. Changfan, Yu-Chin Hsu, Fur-Shing Tsai; "Timing Optimization on Routed Designs with Incremental Placement and Routing Characterization"; IEEE Transactions on computer-Aided Design of Integrated Circuits and Systems; Vol. 19, No. 2; February 2000; pp. 188-196.	
		Amir H. Ajami, Massoud Pedram; "Post-Layout Timing-Driven Cell Placement Using an Accurate Net Length Model with Movable Steiner Points"; ASIA South Pacific DAC; Copyright 2001; pp. 595-600.	
		Konrad Doll, Frank M. Johannes, Kurt J. Antreich; "Iterative Placement Improvement by Network Flow Methods"; IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems; Vol. 13, No. 10; October 1994; pp. 1189-1200.	

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number. ² Applicant is to place a check mark here if English language Translation is attached.

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